Remarks:

This is in response to the final Office Action dated July 2, 2004. The Rule 116 amendment dated November 2, 2004 was not entered. The present amendment replaces the unentered Rule 116 amendment and adds claims 25-35 that were not present in the earlier unentered amendment. Claims 6, 19-22 and 24-35 are pending in this application. Reexamination and reconsideration are respectfully requested.

The final Office Action rejects claim 4. Applicant cancels claim 4 to address this rejection.

The final Office Action rejects claims 19 and 20 over U.S. Patent No. 6,130,452 to Lu, et al. (the Lu patent) taken in view of the IEDM 87 article by Kume, et al., "A Flash-Erase EEPROM cell with an Asymmetric Source and Drain Structure," (the Kume reference). The Office Action rejects claims 21 and 22 over the combination of the Lu patent taken in view of the Kume reference further taken in view of U.S. Patent No. 5,640,345 to Okuda, et al. (the Okuda patent). Claim 6 stands rejected over the combination of the Lu patent taken in view of the Kume reference further taken in view of U.S. Patent No. 5,631,179 to Sung, et al. (the Sung patent). Claim 24 stands rejected over the combination of the Lu patent taken in view of the Kume reference further taken in view of the Okuda patent and still further taken in view of the Sung patent.

The pending claims distinguish over the art cited in the outstanding Office Action and the claims are in condition for allowance.

The present application describes a nonvolatile memory device in which a drain is provided with an overlap to the charge storing floating gate or charge accumulation region. The extent of overlap improves programming. To limit the amount of reduction in the channel length due to the drain overlap and due to the smaller device size, there is little or no overlap between the source and the floating

gate or charge accumulation layer. In the described embodiment (shown in FIG. 3) having a floating gate, the little or no overlap between the source and the floating gate is facilitated by performing erase from the floating gate to the channel region. Finally, the source region is made deeper than the drain region to reduce the resistance of the source region. The art of record does not teach or suggest the structures defined by claims 19 or 21.

The Claimed Programming and Erasing Characteristics Are Physical Claim Limitations

As a preliminary matter, the Office Action at page 5 appears to suggest that the programming and erase characteristics of the claimed memory device are ignored by the Office Action. Specifically the Office Action states:

> "In reference to the claim language referring to how the writing operation is executed, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art."

This statement is inapplicable to the present claims, which are directed to a memory and which implicate the writing and erasing circuitry within the memory. Particular connections must be made to provide the appropriate voltages to the substrate, control gate, source and drain for writing and erasing memory cells in the memory. Due to the number of memory cells within a typical memory, it is not possible to accomplish this on a cell by cell (or block by block) basis by applying signals to the pins of a memory chip. Rather, appropriate connections are provided within the memory. In addition, the write and erase voltages are typically generated on chip to allow the memories to be used in typical systems without unusual supply voltages. Little of the writing, erasing and voltage generation circuitry is illustrated in the application because it is understood by those of

ordinary skill to be present. Nevertheless, different connections and voltage sources are needed to accomplish different writing and erasing and so these writing and erasing aspects of the claims represent physical differences and must be properly analyzed as limitations to these claims.

Consequently, the writing and erasing characteristics of the memory recited in the claims correspond to physical differences between the claimed memory and other memories. To the extent that the final Office Action was based on this erroneous presumption, applicant requests withdrawal of the final Office Action.

Claim 19's Channel Erasing Characteristics Are Not Taught By the Prior Art

The Office Action states at page 3 that the Lu patent describes "the erasing and writing procedures are as claimed (Column 4 Line 27 to Column 5 Line 13) including using hot electron injection (Column 5 Lines 5 to 7)." This statement is incorrect.

Claim 19 recites that "an erasing operation is performed by releasing electrons held by said floating gate into said channel region." As stated, claim 19 provides erase across the channel region, which distributes the erase current over the channel region rather than concentrating the erase current at the edge of the source or drain. The distributed erase procedure limits damage to the dielectric between the floating gate and the channel region in the claim 19 configuration, improving memory lifetime. This erase into the channel of the memory cell is not described in the Lu patent. Nor does the Kume reference address this issues. The Kume reference specifies Fowler-Nordheim tunneling through the source to accomplish erase, which differs from the channel region erase recited by claim 19. Consequently claim 19 and its dependent claims distinguish over the Lu patent taken in view of the Kume reference.

Claim 21's Programming and Erasing Characteristics – Including Erasing by Injecting Holes -- Are Not Taught By the Prior Art

The Office Action states at page 3 that the Lu patent describes "the erasing and writing procedures are as claimed (Column 4 Line 27 to Column 5 Line 13) including using hot electron injection (Column 5 Lines 5 to 7)." This statement is incorrect because the Lu patent and the Kume reference do not describe writing to or erasing an electric charge accumulating portion of an insulating layer. Rather, the teachings are directed to programming or erasing conductive floating gate layers. It is difficult to predict how one might try to implement the devices of the Lu patent and the Kume reference in a memory that provides "an electric charge accumulation portion that is an insulating layer having a trap level therein, said insulating layer being provided between said channel region and control gate," as recited by claim 21. Consequently the combination of the Lu patent and the Kume reference does not teach the programming or erasing strategies of the claim 21 memory.

That the Lu patent and the Kume reference do not teach the erasing operation of claim 21 is further emphasized by the fact that neither the Lu patent nor the Kume reference describes anything about injecting holes into trap levels. That is because these two references teach the strategy of electron tunneling.

The Office Action provides no indication that it relies on the teachings of the Okuda patent for any aspect of the writing or erasing aspects of claim 21. The Okuda patent teaches an entirely different architecture, device and method for writing and erasing a memory cell. The Okuda memory cell provides a capacitor structure with two storage layers separated by a transport layer. Writing values to the Okuda memory cell causes charges to move from one storage layer, across the transport layer to the other storage layer. This is accomplished at low voltages and without any tunneling through the gate dielectric. As such, the writing and erasing

strategies of the Okuda patent are wholly incompatible with those of the Lu patent and the Kume reference.

There is no way to combine the teachings of the Lu patent and the Kume reference, on the one hand, with the teachings of the Okuda patent, on the other hand. This is emphasized in the following passage from column 10, lines 58-65 of the Okuda patent:

> "The semiconductor memory device of the present embodiment does not rely on the F-N current or the hot carrier implantation requiring a high electric field at the time when write/erase operations are executed. Therefore, it is possible to execute write/erase operations at a lower voltage by adjusting carrier capture levels of first and second carrier capture layers 12 and 14."

In other words, the Okuda patent *teaches away* from the write and erase strategies that are taught by the Lu patent and the Kume reference. As such, the Okuda patent does not address the deficiencies of the Lu patent and the Kume reference discussed above.

Thus, claim 21 and its dependent claims distinguish over the combinations cited by the Office Action by reciting: "wherein a writing operation is executed in such a way that hot electrons are generated in the vicinity of said drain region and injected into said electric charge accumulation portion and an erasing operation involves neutralization of the electrons held by the trap level by injecting holes generated in the vicinity of said drain region." None of the art of record teaches or suggests this structure and claim 21 and its dependent claims distinguish over the art of record for this additional reason.

The Lu Patent and the Kume Reference
Do Not Render Obvious the Claimed Source and Drain Configurations

The source and drain structures of the Lu patent are illustrated, for example, in FIG. 8 of the Lu patent. A common source/drain structure is shown, in which the 606a portion of the n+ diffusion is the source region for the transistor including floating gate 404a and the 502a portion of that same n+ diffusion is the drain region for the transistor including floating gate 404b. Because of the common source and drain structures, it is difficult to independent change the characteristics of the source and drain regions of the Lu patent's structure. The Lu patent is directed to just such a difference between the source and drain regions in that the Lu patent makes an asymmetric source/drain structure in which the drain portion 502a extends deeper and further into the channel than does the source region 606b for the transistor including the floating gate 404b. *See* Lu patent, column 8, lines 1-19.

It is *not possible* to modify the Lu patent's source and drain structure to accommodate the teachings of the Kume reference without destroying the advantages the Lu patent sought to gain through its asymmetric structure. The Lu patent seeks to increase the overlap between the drain region 502a and the floating gate 404b. This is accomplished by selective implantation of ions at different energies followed by diffusion during the thick oxide growth to create the illustrated asymmetric common source and drain structures. The depth of the source region 606b in the Lu patent's structures cannot be increased without also increasing the overlap between the source and the floating gate. To make the source of the Lu patent deeper than the drain region, it would be necessary to make the source region extend further into the channel region than the drain region. This is because the depth of the source or drain regions in the Lu patent structure is directly related to the overlap with the channel region because the depth is created by implantation profile and diffusion in the same way as the channel overlap.

Thus, the Lu patent does not teach the limitations of the pending claims and it would not be obvious to modify the Lu patent's structure to make the source region deeper than the drain region.

That it would not be possible to modify the Lu patent's teachings to produce the present application's invention is *emphasized* by the Kume reference. As shown in its FIG. 1, the Kume reference describes a source region that overlaps the channel region further than the drain region – as a natural consequence of making the source region deeper than the drain region. Each of these source and drain regions is formed through diffusion and the Lu patent's structure and the Kume reference's structure cannot avoid the consequence that diffusing the source region to a depth lower than the drain region also causes the source region to overlap further into the channel region.

None of the other references change this analysis. Consequently, nothing in the cited art teaches or suggests the source and drain structure defined in the pending claims. Consequently, claim 19 and its dependent claims distinguish over the cited combination by reciting "wherein an overlap of said drain region with said floating gate is larger than an overlap of said source region with said floating gate ...[and] wherein a junction depth of said source region is larger than a junction depth of said drain region."

Similarly, claim 21 and its dependent claims distinguish over the cited art by reciting "wherein an overlap of said drain region with said electric charge accumulating portion is set larger than an overlap of said source region with said electric charge accumulating portion; and wherein a junction depth of said source region is larger than a junction depth of said drain region."

In view of the foregoing, applicant respectfully submits that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6742 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: December 30, 2004

By: _____
William H. Wright
Registration No. 36,312
Attorney for Applicant(s)

500 South Grand Avenue, Suite 1900
Los Angeles, California 90071
Phone: 213-337-6700
Fax: 213-337-6701